AMENDMENT UNDER 37 C.F.R. 1.116 - EXPEDITED PROCEDURE

Serial Number: 09/476622 Filing Date: December 31, 1999 Title: EXTERNAL MICROCODE Assignee: Intel Corporation Page 6 Dkt: 884.101US1 (INTEL)

## REMARKS

This communication is filed in response to the Office Action mailed on October 22, 2003. No claims are amended, no claims are canceled, and no claims are added. As a result, claims 10 and 21-40 are now pending in this Application.

# §112 Rejection of the Claims

Claim 37 was rejected under 35 USC § 112, first paragraph, as failing to comply with the written description requirement. Since a *prima facie* case for non-enablement under § 112, first paragraph, has not been established, and since the specification in the Application does indeed provide enablement commensurate with the scope of claim 37, this rejection is respectfully traversed.

The specification in an application need only describe the invention to one of ordinary skill in the art. As explained by the Federal Circuit:

Requiring inclusion in the patent of known scientific/technological information would add an imprecise and open-ended criterion to the content of patent specifications, could greatly enlarge the content of patent specifications and unnecessarily increase the cost of preparing and prosecuting patent applications, and could tend to obfuscate rather than highlight the contribution to which the patent is directed. A patent is not a scientific treatise, but a document that presumes a readership skilled in the field of the invention. *Ajinomoto Co., Inc. v. Archer-Daniels-Midland Co.* 56 USPQ 2d 1332, 1338 (Fed. Cir. 2000).

As described in MPEP § 2164 et seq., the burden is on the Examiner to establish a *prima* facie case to maintain a rejection of non-enablement with respect to the disclosure of a patent application under 35 U.S.C. § 112, first paragraph. Such a case requires:

- 1. a rational basis as to
  - a. why the disclosure does not teach, or
  - b. why to doubt the objective truth of the statements in the disclosure that purport to teach;
- 2. the manner and process of making and using the invention;
- 3. that correspond in scope to the claimed invention;
- 4. to one of ordinary skill in the pertinent technology;

Serial Number: 09/476622 Filing Date: December 31, 1999 Title: EXTERNAL MICROCODE Assignee: Intel Corporation

- 5. without undue experimentation; and
- 6. dealing with subject matter that would not already be known to the skilled person as of the filing date of the application.

"The Examiner must provide evidence ... supporting each of these elements for a rejection under the first paragraph of § 112 to be proper." See *Patent Prosecution, Practice and Procedure Before The United States Patent Office*, Ira H. Donner, pg. 691, 2002.

First, according to a statement made by the Examiner in the instant Office Action, "While the examiner might readily acknowledge any idiot in the art might have the knowledge and motivation to use the processor and something like EEPROM to modify the external microcode, this has never been part of the applicants' written disclosure ...". This appears to be an explicit admission by the Office that the specification is in accordance with the requirement that "35 U.S.C. 112 requires the specification to be enabling only to a person "skilled in the art to which it pertains, or with which it is most nearly connected. ... The specification need not disclose what is well-known to those skilled in the art and preferably omits that which is well-known to those skilled and already available to the public." *In re Buchner*, 929 F.2d 660, 661, 18 USPQ2d 1331, 1332 (Fed. Cir. 1991); *Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 1384, 231 USPQ 81, 94 (Fed. Cir. 1986), *cert. denied*, 480 U.S. 947 (1987); and *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1463, 221 USPQ 481, 489 (Fed. Cir. 1984)."

Second, as part of establishing a prima facie case of non-enablement, the Office must demonstrate that one of ordinary skill in the pertinent technology would not be able to practice the invention without undue experimentation, in light of what would be known to the skilled person as of the filing date of the application. This has not been accomplished.

Mere assertions regarding a lack of detail in the specification, without any attempt to show that the missing information requires undue experimentation by one of ordinary skill in the art, given the state of the art at the time the Application was filed, are not effective to meet the standard set forth in MPEP § 2164 et seq.

The *prima facie* case of non-enablement requires a showing of the six elements outlined previously: (1) why the disclosure fails to teach, or why teachings therein should be doubted, (2) why the manner and process making/using the invention isn't taught, (3) why teachings don't

Serial Number: 09/476622 Filing Date: December 31, 1999 Title: EXTERNAL MICROCODE

Assignee: Intel Corporation

correspond in scope to the claimed invention, (4) why one of ordinary skill would not comprehend the teachings, (5) why undue experimentation would be necessary, and (6) why the subject matter not disclosed would not already be known skilled person in the art. All of these elements must be shown, as of the filing date of the Application. The various assertions made in the Office Action do not serve to demonstrate each of these required points.

Third, it is respectfully noted that claim 37 reads as follows:

The article of claim 35, wherein the machine-accessible medium further includes data, which when accessed by the machine, results in the machine performing: reprogramming the microcode in the firmware.

The "machine" noted therein is not necessarily the "processor" of claim 35. It may be another processor or some other machine capable of accessing data and performing various activities as a result. Thus, it is improper to characterize claim 37 as being limited to a set of circumstances where "... the processor modifies the external microcode firmware where previously the firmware was only modified without the agent of change being identified", and the Applicants respectfully request that no such limitation be placed on claim 37.

Therefore, because the Office admits the specification has been formulated in accordance with the requirements of 35 U.S.C. § 112, as interpreted by caselaw, and because the Office has not established a *prima facie* case of non-enablement under 35 U.S.C. § 112, first paragraph, as required by MPEP § 2164, the Applicants respectfully request reconsideration and withdrawal of this rejection under § 112.

## §102 Rejection of the Claims

Claims 10, 21, 23-24 and 38-40 were rejected under 35 USC § 102(e) as being anticipated by Mahalingaiah et al. (U.S. 6,141,740, hereinafter "Mahalingaiah"), incorporating Witt (U.S. 5,623,619, hereinafter "Witt") by reference. Claims 21-22 and 35-36 were rejected under 35 USC § 102(b) as being anticipated by Dao et al. (U.S. 4,928,223, hereinafter "Dao"). The Applicants do not admit that Mahalingaiah or Dao are prior art and reserve the right to swear behind any of these references at a later date. In addition, because the Applicants assert that the

### AMENDMENT UNDER 37 C.F.R. 1.116 - EXPEDITED PROCEDURE

Serial Number: 09/476622 Filing Date: December 31, 1999 Title: EXTERNAL MICROCODE Assignee: Intel Corporation

Office has not shown that Mahalingaiah or Dao disclose the identical invention as claimed, the Applicants respectfully traverse this rejection of the claims.

Anticipation under 35 USC § 102 requires the disclosure in a single prior art reference of each element of the claim under consideration. *In re Dillon* 919 F.2d 688, 16 USPQ 2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim*." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). "The *identical invention* must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131 (emphasis added).

It is respectfully noted that the structure of Mahalingaiah does not permit execution of microcode in the same manner as is taught by the Applicants. For example, while the Application describes embodiments wherein "one or more functions of the processor are controlled ... by directly triggering hardware on the processor", Mahalingaiah notes that "... complex instructions are classified as MROM instructions. MROM instructions are transmitted to a microcode unit within the microprocessor, which ... produces two or more ... microcode instructions for execution by the microprocessor." See Mahalingaiah, Col. 2, lines 8-13. The microcode of Mahalingaiah is only fetched from external memory when an MROM instruction is encountered that translates into a plurality of microcode instructions. *Id.* at Col. 16, lines 12-21. Since Mahalingaiah requires each MROM instruction to translate into "two or more ... microcode instructions" it would be impossible to execute a single microcode instruction at will using the apparatus disclosed by Mahalingaiah.

Further, "[L]ess complex instructions are decoded by hardware decode units within the microprocessor, without intervention by the microcode unit. The terms 'directly decoded instruction' and 'fastpath instruction' will be used herein to refer to instructions which are decoded and executed by the microprocessor without the aid of a microcode unit ... directly-decoded instructions are decoded and executed via hardware decode and functional units

Serial Number: 09/476622 Filing Date: December 31, 1999 Title: EXTERNAL MICROCODE Assignee: Intel Corporation

included within the microprocessor." Id. at Col. 2, lines 37-45. Thus, it is the "directly decoded" instructions of Mahalingaiah that correspond to the "microcode" of the instant Application, and these directly decoded instructions of Mahalingaiah are not stored in external memory.

It is also respectfully noted that Dao does not define microcode in the same way as the Applicants. Dao teaches the existence of macrocode, microcode, and nanocode. See Dao, Col. 1, line 63 - Col. 2, line 8. While the existence of an external microcode read only memory (ROM) is noted, it has its own local bus. Use of a main memory bus, as claimed by the Applicants, is specifically avoided. Further, it is noted that the microcode instruction merely defines the starting point of a nanocode instruction sequence. Id. at Col. 35, lines 19-21. The arithmetic logic unit (ALU) handles nanocode sequencing, and not microcode sequencing. Id. at Col. 37, lines 42-55. Thus, it is the "nanocode" instructions of Dao which equate to the terms "microcode" functions and "programmed code" used by the Applicants, and these nanocode instructions of Dao are not stored in external memory, but in a ROM and a programmable logic array integral with the ALU. Id., Figs. 2 and 15, and Col. 7, lines 3-25.

Therefore, since neither Mahalingaiah nor Dao teach directly executable microcode stored in external memory, what is disclosed by these references is not identical to the subject matter of the embodiments claimed, and therefore, the rejection of claims 10, 21, 21-24, 35-36, and 38-40 under § 102 is improper. Reconsideration and allowance is respectfully requested.

## §103 Rejection of the Claims

Claim 10 was rejected under 35 USC § 103(a) as being unpatentable over Shiraogawa (U.S. 4,131,943, hereinafter "Shiraogawa"). Claim 37 was also rejected under 35 USC § 103(a) as being unpatentable over Dao. First, the Applicants do not admit that Shiraogawa or Dao are prior art and reserve the right to swear behind these references in the future. Second, since a prima facia case of nonobviousness has not been established in each case, as required by M.P.E.P. § 2142, the Applicants respectfully traverse these rejections.

No proper prima facie case of obviousness has been established because (1) combining the references does not teach all of the limitations set forth in the claims, (2) there is no

Serial Number: 09/476622 Filing Date: December 31, 1999 Title: EXTERNAL MICROCODE Assignee: Intel Corporation

motivation to combine the references, and (3) combining the references provides no reasonable expectation of success. Each of these points will be explained in detail, as follows.

First, with respect to claim 10, the Office admits that "Shiraogawa did not specifically mention storing his macroinstruction ... programs in an external, computer-readable medium." No other references are mentioned to combine with Shiraogawa, and therefore nothing in the record serves to supply this deficiency. As a result, no reasonable expectation of success arises.

Second, the Examiner offers to take "Official Notice of the fact that storage of macroinstruction/machine-instruction programs in external media is well known in the art. On of ordinary skill is motivated to store such programs externally to conserve valuable internal chip real estate." However, these bare assertions are unsupported by evidence in the record, and in fact are negated by the showing above that neither Mahalingaiah nor Dao above demonstrate the precise type of storage claimed by the Applicants. The use of such unsupported assertions in the Office Action does not satisfy the explicit requirements needed to demonstrate motivation as set forth by the *In re Sang Su Lee* court. Thus, the Examiner appears to be using personal knowledge, and is respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

With respect to dependent claim 37, the Office admits that "Dao ... did not specifically teach the processor modifying the microcode firmware ...". No other references are mentioned to combine with Dao, and therefore nothing in the record serves to supply this deficiency. As a result, no reasonable expectation of success arises.

Second, the Examiner offers to take "Official Notice of the fact that firmware storage that is readily modifiable by a processor was prevalent at the time of applicants' invention. Dao would have been motivated to use it to store and revise his microcode because it is readily modifiable given the frequency with which one typically modifies microcode but is also relatively secure from tampering by the incompetent." However, these bare assertions are unsupported by evidence in the record, and in fact are negated by the showing above that Dao does not demonstrate the precise type of storage claimed by the Applicants. The use of such unsupported assertions in the Office Action does not satisfy the explicit requirements needed to demonstrate motivation as set forth by the *In re Sang Su Lee* court. Thus, the Examiner appears

Dkt: 884.101US1 (INTEL)

Serial Number: 09/476622 Filing Date: December 31, 1999 Title: EXTERNAL MICROCODE Assignee: Intel Corporation

to be using personal knowledge, and is respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

Therefore, since there is no evidence in the record to support disclosure by either Shiraogawa or Dao of the admitted missing elements in claims 10 and 37, since there is no motivation to supply the missing elements, and since no reasonable expectation of success arises, a *prima facie* case of obviousness has not been established. This conclusion applies with even greater force respecting dependent claim 37, since any claim depending from a nonobvious independent claim is also nonobvious. See M.P.E.P. § 2143.03. It is therefore respectfully requested that the rejections of claims 10 and 37 under 35 U.S.C. § 103 be reconsidered and withdrawn.

AMENDMENT UNDER 37 C.F.R. 1.116 - EXPEDITED PROCEDURE

Serial Number: 09/476622 Filing Date: December 31, 1999 Title: EXTERNAL MICROCODE Assignee: Intel Corporation

#### Page 13 Dkt: 884.101US1 (INTEL)

### CONCLUSION

The Applicants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, Mark Muller, at (210) 308-5677, or Applicants' below-named representative at (612) 349-9592 to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

HOWARD CHIN ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. Attorneys for Intel Corporation P.O. Box 2938
Minneapolis, Minnesota 55402
(612) 349-9592

Date Dec. 16 2003

Ann M. McCrackin Reg. No. 42,858

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this day of December, 2003.

KACIA LEE

Signature

Name